MULTI-BIT NON-VOLATILE MEMORY DEVICE AND METHOD THEREFOR

ABSTRACT

A multi-bit non-volatile memory device includes a charge storage layer (14) sandwiched between two insulating layers (12 and 16) formed on a semiconductor substrate (10). A thick oxide layer (18) is formed over the charge storage layer (14) and a minimum feature sized hole is etched in the thick oxide layer (18). An opening is formed in the thick oxide layer (18). Side-wall spacers (60) formed on the inside wall of the hole over the charge storage layer have a void (62) between them that is less than the minimum feature size. The side-wall spacers (60) function to mask portions of the charge storage layer (14), when the charge storage layer is etched away, to form the two separate charge storage regions (55 and 57) under the side-wall spacers (60). The device can be manufactured using only one mask step. Separating the charge storage regions prevents lateral conduction of charge in the nitride.